Joint Inventors

Docket No. 20063/10022

"EXPRESS MAIL" mailing label No.
EV 403728139 US
Date of Deposit: **December 31, 2003**

I hereby certify that this paper (or fee) is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR §1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that We, **Chang Hun HAN**, a citizen of the Republic of Korea, residing at #101-605 Hyundai 1-cha Apt., Changjeon-dong, Icheon-si, Gyeonggi-do 467-731, Korea; and **Bong Kil KIM**, a citizen of the Republic of Korea, residing at 332 Choi-dong, Hanam-si, Gyeonggi-do 465-220, Korea have invented a new and useful **METHOD FOR FABRICATING AND-TYPE FLASH MEMORY CELL**, of which the following is a specification.

METHOD FOR FABRICATING AND-TYPE FLASH MEMORY CELL

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to a method for manufacturing an AND type flash memory device.

BACKGROUND

[0002] In fabricating a flash memory device, the cell array is an important factor determining a type of a flash memory device together with a memory device structure, an erasing method, and a programming method. Among various cell array structures, AND-type cell arrays can embody the density and the high-performance operation of a flash memory.

[0003] Fig. 1 is a schematic diagram illustrating a cell array of a conventional AND-type flash memory device. The conventional AND-type flash memory device embodies densification (i.e., greater density) by sharing bit line contacts and source lines in a plurality of cells and suppresses the occurrence of disturbances during program operation through parallel connection and the layered bit lines and source lines. However, a conventional AND-type flash memory device has a shortcoming in that interconnection density in a diffusion layer is high.

[0004] Figs. 2a through 2h illustrate, in cross-sectional views, the fabricating process of an AND-type flash memory device according to a conventional method. Referring to Fig. 2a, a pad oxide layer 13 and a pad nitride layer 15 are deposited in sequence on a silicon substrate 11. Then, a photoresist pattern 15 is formed on the pad nitride layer 15.

[0005] Referring to Fig. 2b, some part of the pad nitride layer 15, the pad oxide layer 13, and the substrate 11 is removed by an etching process using the photoresist pattern 17 as a mask. As a result, a pad oxide pattern 13a and a pad nitride pattern 15a

are formed on the substrate 11 and a trench 19 with a predetermined depth is formed in the substrate 11.

[0006] Referring to Fig. 2c, the photoresist pattern 17 is removed. Then, a gap filling oxide layer 21 is deposited on the pad nitride pattern 15a and in the trench 19 to fill completely the trench 19.

[0007] Referring to Fig. 2d, an etching process is performed until the pad nitride pattern 15a is exposed to planarize the gap filling oxide layer 21.

[0008] Referring to Fig. 2e, the pad nitride pattern 15a, the pad oxide pattern 13a, and the top portion of the gap filling oxide layer 21a are removed to form a trench isolation layer 21b. Then, a nitride layer 23 for a hard mask is formed on the resulting substrate.

[0009] Referring to Fig. 2f, a mask pattern 25 to form junction regions is formed on the nitride layer 23.

[0010] Referring to Fig. 2g, an ion implantation process is performed using the mask pattern 25 as a mask to form N+ junction regions 27a and 27b in the substrate 11. The ion implanted is preferably As or phosphorus (P).

[0011] Referring to Fig. 2h, the mask pattern 25 and the nitride layer 23 are removed. Then, a floating gate (not shown) is formed on the substrate and an oxide-nitride-oxide (ONO) layer is deposited.

[0012] Consequently, as shown Fig. 5, an AND-type flash memory cell comprising a floating gate oxide 50, a floating gate 55, a control gate oxide 60, and a control gate 65 is completed.

[0013] However, in fabricating an AND-type flash memory cell, the conventional method has to apply twice an exposure process using deep ultraviolet (hereinafter referred to as "DUV") to form a mask for a trench and a mask for N+ junction

regions. In addition, a mask overlap margin is necessarily required due to the two mask processes, thereby causing an increase in cell size. In detail, in order to ensure an appropriate width (XB in Fig. 4) of junction regions, a margin has to be considered to address the misalignment of the mask toward the trench isolation layer and, therefore, cell size increases due to such a margin.

[0014] Moreover, with the high-integration of a semiconductor device, a junction region in a substrate has to have a width less than 0.25μm. Such a length can be formed only through a process using DUV wavelength or a higher wavelength than that. However, a mask process using DUV may increase manufacturing costs due to a high photoresist price and reticle making costs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Fig. 1 is a schematic diagram illustrating the cell array of a conventional AND-type flash memory device.

[0016] Figs. 2a through 2h illustrate, in cross-sectional views, the fabricating process of an AND-type flash memory device according to a conventional method.

[0017] Fig. 3 is a schematic diagram illustrating the cell array of an example AND-type flash memory device.

[0018] Fig. 4 is a layout of an example AND-type flash memory cell.

[0019] Fig. 5 is a perspective view of an example AND-type flash memory cell.

[0020] Figs. 6a through 6i illustrate, in cross-sectional views, the fabricating process of an example AND-type flash memory cell.

DETAILED DESCRIPTION

[0021] As described in detail below, an example method for fabricating an AND-type flash memory provides a high-integration of interconnection density in a diffusion layer by forming self-aligned junctions in a substrate. More specifically, an example method for fabricating an AND-type flash memory cell depositis a pad oxide layer and a pad nitride layer on a silicon substrate, removes some part of the pad nitride layer to form a pad nitride layer pattern, implants ions into the substrate to form ion implant regions, forms spacers on the sidewalls of the pad nitride layer pattern, removes some part of the pad oxide layer and the top portion of the substrate through an etching process using the spacers as a mask to form a trench, which divides the ion implant region into two parts. In addition, the example method forms a gap filling insulating layer over the resulting substrate, and forms a trench isolation layer and junction regions simultaneously by removing the spacers, the pad nitride layer pattern, the pad oxide layer, and the top portion of the gap filling insulating layer.

[0022] Referring to Fig. 3, in an example AND-type flash memory cell, one of junction regions positioned between device isolation layers is shared between two cells in order to embody densification of a diffusion layer. Figs. 4 and 5 illustrate, in a layout and a perspective view, such an array structure of the AND-type flash memory device.

[0023] Referring to Fig. 6a, a pad oxide layer 33 and a pad nitride layer 35 are deposited in sequence on a substrate 31. Then, a photoresist pattern 37 is formed on the pad nitride layer 35.

[0024] Referring to Fig. 6b, some part of the pad nitride layer 35 is removed through an etching process using the photoresist pattern 37 as a mask. As a result,

some part of the pad oxide layer 33 is exposed. Then, the photoresist pattern 37 is removed.

[0025] Referring to Fig. 6c, ions are implanted into the substrate 31 to form ion implant regions 39 and 41. The implanted ions are preferably As ion or P. Here, the pad oxide layer 33 functions as a screen oxide layer to prevent damage of the silicon substrate during the ion implantation.

[0026] Referring to Fig. 6d, an insulating layer 43 is deposited over the resulting substrate 31. The insulating layer 43 is preferably between 500Å and 1500Å in thickness and is preferably formed of a material selected from the group consisting of nitride and TEOS (tetraethyl orthosilicate) oxides.

[0027] Referring to Fig. 6e, some part of the insulating layer 43 is removed to form spacers 43a on sidewalls of the pad nitride layer pattern 35a.

[0028] Referring to Fig. 6f, the exposed pad oxide layer 33 and the top portion of the silicon substrate 31 between the both spacers 43a are removed to form a trench 45 for device isolation. At the same time, the ion implant region 39 is divided into two parts and the implant region 39a under the spacers 43a remains as it is. The trench 45 and the ion implant region 39a are formed in a self-aligned manner.

[0029] Referring to Fig. 6g, a gap filling insulating layer 47 is deposited over the resulting substrate 31. Next, a thermal treatment for the densification of the gap filling insulating layer 47 and the activation of the ion implant region may also be performed.

[0030] Referring to Fig. 6h, a chemical mechanical polishing (CMP) or an etch back process is performed for the gap filling insulating layer 47 to separate cells.

[0031] Referring to Fig. 6i, the spacers, the pad nitride layer pattern, the pad oxide layer, and the top portion of the gap filling insulating layer are removed. As a result, junction regions 39a and 41 and a trench isolation layer 47a are formed in the substrate 31.

[0032] The example memory structures described herein can embody high-integration by forming self-aligned device isolation layers and junction regions simultaneously while fabricating an AND-type flash memory cell. In addition, the example fabrication methods described herein can reduce manufacturing costs by omitting one of two mask processes using DUV.

[0033] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.